Translation

PCT/DE2002/004521

PATENT COOPERATION TREATY

PCT

Patentanwaltskanzlei Kindermann

06. Sep. 2004

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INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference In1222WO	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/DE2002/004521	International filing date (*day/month/year*) 10 December 2002 (10.12.2002)	Priority date (*day/month/year*) 15 January 2002 (15.01.2002)
International Patent Classification (IPC) or national classification and IPC H01L 27/115, 21/8246, 27/105, 21/8247		
Applicant INFINEON TECHNOLOGIES AG		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

☒ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

These annexes consist of a total of 2 sheets.

3. This report contains indications relating to the following items:

- I ☒ Basis of the report
- II ☐ Priority
- III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- IV ☐ Lack of unity of invention
- V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- VI ☐ Certain documents cited
- VII ☐ Certain defects in the international application
- VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
26 July 2003 (26.07.2003)	04 June 2004 (04.06.2004)
Name and mailing address of the IPEA/EP Facsimile No.	Authorized officer Telephone No.

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/DE2002/004521

I. Basis of the report

1. With regard to the **elements** of the international application:*

☐ the international application as originally filed

☒ the description:
pages 1-13, as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____

☒ the claims:
pages 2-7, 9-16, as originally filed
pages _____, as amended (together with any statement under Article 19
pages _____, filed with the demand
pages 1, 8, filed with the letter of 16 January 2004 (16.01.2004)

☒ the drawings:
pages 1-4, as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____

☐ the sequence listing part of the description:
pages _____, as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in written form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☐ The amendments have resulted in the cancellation of:

☐ the description, pages _____

☐ the claims, Nos. _____

☐ the drawings, sheets/fig _____

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rule 70.16 and 70.17).*

*** Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/DE 02/04521

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims		YES
	Claims	1, 2, 4-7	NO
Inventive step (IS)	Claims		YES
	Claims	3, 8-16	NO
Industrial applicability (IA)	Claims	1-16	YES
	Claims		NO

2. Citations and explanations

1. This report makes reference to the following document:

D1: EP-A-1 102 319

2. D1 is regarded as the prior art closest to the subject matter of claims 1 and 8. That document discloses (see paragraphs 16-24, 27 and 28 and figures 8-20) a nonvolatile two-transistor semiconductor memory cell 82 having a memory transistor 84 with a predetermined threshold voltage and a selection transistor 83 with a predetermined threshold voltage, the selection transistor control layer 43c having a different make-up than the charge storage layer 27d.

D1 can also be interpreted as the two threshold voltages in the selection and storage transistors being increased by increased substrate/well doping (see paragraph 12, in particular column 3, line 1).

The phrase "in order to correct the threshold value increase" is not sufficient for distinguishing the

from D1.

The subject matter of claim 1 is therefore not novel (PCT Article 33(2)).

3. Dependent claims 2 and 4 to 7 do not contain any features which, in combination with the features of any claim to which they refer, meet the PCT requirements with regard to novelty and inventive step.

4. The subject matter of claim 3 differs from the memory cell known from D1 in that the semiconductor layer (4) has doping of the first conduction type (p) in a region of the selection transistor. However, this feature has already been used for the same purpose in a similar MOS transistor (see D1, in particular paragraph 27). D1 describes the same advantages as the present application. A person skilled in the art would therefore regard the incorporation of this feature into the memory cell described in D1 as a conventional measure for solving the stated problem. The subject matter of claim 3 therefore does not involve an inventive step (PCT Article 33(3)).

5. The subject matter of claim 8 differs from the method known from D1 (see also paragraph 12) in that the semiconductor layer (4) has doping of the first conduction type (p) in a region of the selection transistor. As mentioned in point 4, this feature has already been used for the same purpose in the similar MOS transistor 80 (see D1, in particular paragraph 27). The subject matter of claim 8 therefore does not involve an inventive step (PCT Article 33(3)).

6. Dependent claims 9 to 16 do not appear to contain any features which, in combination with the features of any claim to which they refer, meet the PCT requirements with regard to novelty and inventive step.

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DT11 Rec'd PCT/PTO 13 JUL 2004
PCT/DE02/04521

New Patent Claims 1 and 8

1. Nonvolatile two-transistor semiconductor memory cell having

a memory transistor (ST) having a predetermined threshold voltage, which has a source and drain region (2) with a channel region lying in between in a substrate (1), a first memory transistor insulation layer (3), a charge storage layer (4), a second memory transistor insulation layer (5) and a memory transistor control layer (6) being formed at the surface of the channel region; and

a selection transistor (AT) having a predetermined threshold voltage, which has a source and drain region (2) with a channel region lying in between in the substrate (1), a first selection transistor insulation layer (3') and a selection transistor control layer (4*) being formed at the surface of the channel region, characterized in that

the two threshold voltages in the selection and memory transistors (AT, ST) are raised by an increased substrate/well doping and, for correction of the threshold raising in the selection transistor (AT), the selection transistor control layer (4*) is formed differently from the charge storage layer (4).

8. Method for fabricating a nonvolatile two-transistor semiconductor memory cell having the following steps:

a) formation of a first insulation layer (3, 3') for a selection transistor (AT) having a predetermined threshold voltage and a memory transistor (ST) having a predetermined threshold voltage on a semiconductor substrate (1), which has a doping of the first conduction type (p);

b) formation of a semiconductor layer (4) at the surface of the first insulation layer (3, 3');

c) formation of a second insulation layer (5) at the surface of the electrically conductive semiconductor layer (4) at least in the region of the memory transistor (ST);

d) formation of a further electrically conductive layer (6) at the surface of the second insulation layer (5) at least in the region of the memory transistor (ST);

e) formation and patterning of a mask layer (7);

f) formation of layer stacks in the region of the selection transistor (AT) and of the memory transistor (ST) using the patterned mask layer (7); and

g) formation of source and drain regions (2) with a doping of the second conduction type (n) using the layer stack as mask, in which case

in step a), the two threshold voltages in the selection and memory transistors (AT, ST) are raised by an increased doping of the semiconductor substrate (1), and

in step b), for correction of the threshold raising in the selection transistor (AT), the semiconductor layer (4) has a doping of the first conduction type (p) in a region of the selection transistor (AT) and a doping of the second conduction type (n), which doping is opposite to the first conduction type, in a region of the memory transistor (ST).